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Efficient VLSI Architecture for CMOS Image Sensor with Reconfigurable Array Processing

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Abstract: *Digital CMOS Image Sensor (CIS) are an attractive emerging technology. It is possible to use cameras and other imaging system. Several vlsi architecture have been proposed like active pixel sensor and passive pixel sensor and CCD. They have some limitation in architecture and dynamic range and SNR and resolution level. This paper presents a CMOS image sensor (CIS) VLSI architecture based on reconfigurable PWM and array processing. Resolution in the image sensor will be depends upon the no of pixel in the array format. Array format can be used 512x512 pixels, 256x256 pixels, 128x128 and also 64x64 pixels. The presented VLSI architecture for CMOS Image sensor can perform all above mentioned array format. This architecture achieves higher dynamic range and good SNR and also various resolution based image can be obtained. High readout capability obtained.*

Keyword: *Image Sensor, Reconfigurable PWD, Dynamic Range.*

1. Introduction

TO GAIN an economic advantage in the crowded solid state image sensor arena, last decade has seen numerous approaches toward formulation of new architectures for implementation of CMOS image sensor (CIS) technology. It is possible to use cameras and other imaging system. CMOS technologies allowed to dramatically reducing the cost of digital cameras, which are nowadays ubiquitous in everyday life. However, there are always new challenges for the image-sensor research community, and three-dimensional (3D) imaging is undoubtedly one of the emerging topics due to the urgent requirements from many consumer applications, e.g. ambient-assisted living, automotive, gaming and virtual reality, etc. The charge-coupled device (CCD) technology have been the dominant tool for electronic image sensors for several decades due to their high photosensitivity, low fixed pattern noise (FPN), small pixel, and large array sizes. However, in the last decade, complimentary metal–oxide–semiconductor (CMOS) image sensors have gained attention from many researchers and industries due to their low energy dissipation, low cost, on chip processing capabilities, and their integration on standard or quasi-standard very large scale integration (VLSI) process. Still, raw output images acquired by CMOS sensors present poor quality for display and need further processing, mainly because of noise, blurriness, and poor contrast. In order to tackle these problems, image processing circuits are typically associated with image sensors as a part of the whole vision system Optical range image capturing techniques are superior to other non-optical methods (e.g. ultrasonic, radar, etc.) in terms of speed and lateral resolution and will be described in the following. Optical distance measurement can be classified, with respect to the employed physical principle, into three categories: interferometry, triangulation and time-of-flight (TOF) [1]. On the other hand, interferometric systems require precise optical setup, and the depth range is very limited [2]. Range cameras based on time-of-flight technique, both indirect and direct; extract the distance measurement by sensing the delay between the light emitted from an illuminator and the same light backscattered towards the sensor by the target. The digital CMOS image sensor should be good DR, SNR, and fill factor. In photography, dynamic range is the range between the maximum and minimum measurable light intensities. The varying degree of light intensity depends on the device that is used as a capture device, which decides the overall performance of a dynamic range of an imaging sensor.

The existing system describes architecture of CMOS image sensor based on time to threshold. The approach pursued in CISs based on pulse width modulation (PWM) architecture incorporates a CMOS inverter as a comparator within a pixel. The technique creates additional pixel area allowing for the incorporation of additional processing circuitry [3]. The limitation may emerge as the result of: 1) the dependency of power consumption on the light variation. For example, at dark light, the very slow change in voltage during the integration phase at the PD node and the inverter will cause an increase in short-circuit power consumption and 2) response of the imager is not a linear function with variation of illumination intensity.

The proposed system describes architecture of CMOS image sensor with reconfigurable array processing for various resolutions by the architecture. You may or may not need lots of resolution, depending on what you want to do with your pictures. If you are

planning to do nothing more than display images on a Web page or send them in e-mail, then using 640x480 resolution has several advantages: Your camera's memory will hold more images at this low resolution than at higher resolutions. It will take less time to move the images from the camera to your computer. The images will take up less space on your computer. On the other hand, if your goal is to print large images, you definitely want to take high-resolution shots and need a camera with lots of pixels. The architecture can reconfigurable for various resolution.

This paper is organized as follows. Introduced the new CIS architecture based on reconfigurable array processing is described in Section II. This is followed by Section III whereby focus is directed toward the experimental results and CIS characterization, and finally, Section IV provides the concluding remarks.

2. Cmos Digital Imager Logical Architecture

2.1. Reconfigurable PWM Imager Architecture

The logical architecture for the reconfigurable PWM imaging system is shown in Figure 1. It includes PWM pixel array, control circuits, i.e. signal circuitry generator row decoder and column decoder. The PWM array consist M x N CIS array, a pixel *Pi, j* is in readout mode when the row signal reset_i is low and the row enable i is high.

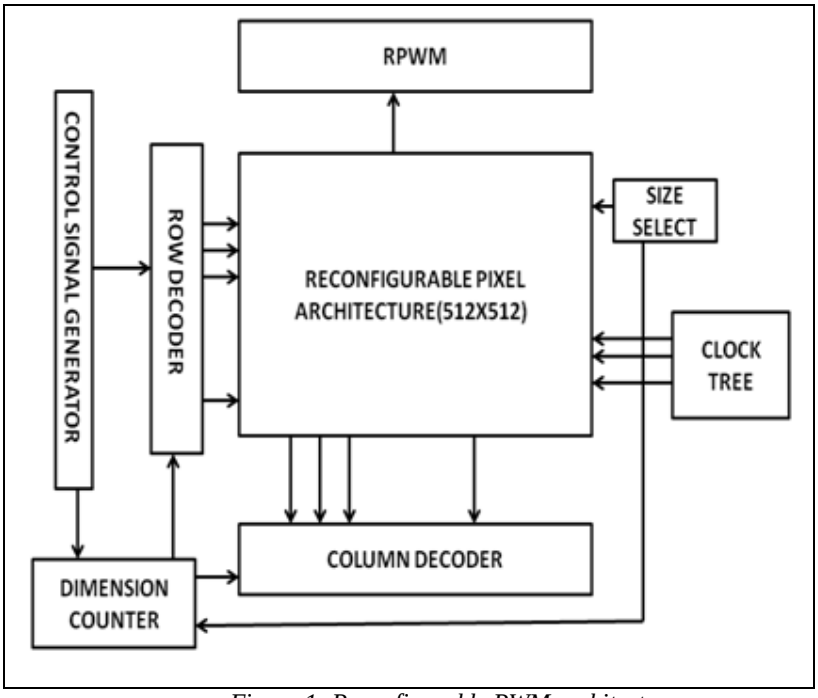

Figure 1: Reconfigurable PWM architecture

2.2. Single pixel in CIS imager

The pixel-based CIS architecture uses a single-inverter sensor circuitry. The basic pixel structure shown in Fig. 3(a) includes a PD, a single CMOS inverter, two reset nMOS transistors M1 and M2, and the two nMOS transistors M3 and M4 to enable the pixel output. The operation is initiated with the reset signal being asserted. Node PD [Fig. 2(a)] commences to charge up toward +*V*DD, followed by the integration phase whereby the reset is switched to logic 0 and the enable signals is switched logic 1. The PD enters a floating mode during this period. Upon illumination on PD. Local variations in threshold voltage are not negligible, and can cause differences in performance between two neighboring pixels. The differences between the individual pixels in the array result in variations in the analog readout, which culminates in the fixed

pattern noise (FPN). The two important sources of errors are: 1) variation in gain and 2) offset of the comparator. Because the gain in the comparator is large, the local gain variation will have a minor effect.

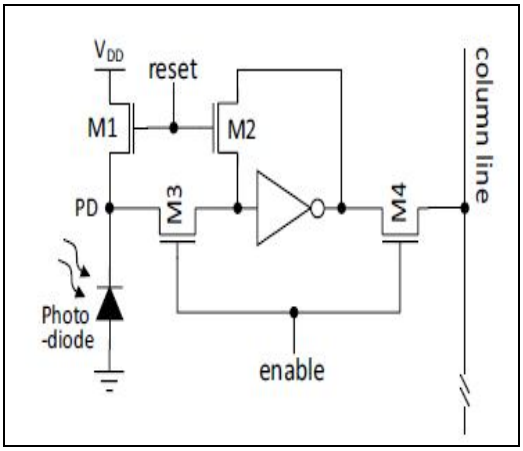

Figure 2: Pixel architecture based on utilization of a single-inverter CIS

2.3. DR and SNR

Two of the most important parameters of image sensors are the signal-to-noise ratio (SNR) and the dynamic range (DR).

SNR is a very broad way to determine image sensor quality. For a given imaging scene and exposure, a higher SNR value will result better image quality. The SNRMAX (see Equation 1) is a logarithmic ratio of signal electrons at the sensor's saturation exposure (NMAX) to either the total or temporal noise in units of electrons. The result is expressed in units of dB.

$$SNRMAX=20\cdot\log10\ (NMAX/n)$$

Equation 2: Formula for signal-to-noise ratio (SNR)

Alternatively, DR is a measure of ratio of the highest and lowest possible signals that can be measured by the sensor (see Equation 3).

$$DR=20\cdot\log10\ (NMAX/nread\ )$$

Equation 3: Formula for dynamic range (DR)

The read noise is the lowest measureable signal, and is defined by the base noise level of the sensor's whole signal chain / system. The DR result is also expressed in units of dB.

3. Simulation Result

The proposed architecture can be simulated using MATLAB and ModelSim 6.4, and result related to various threshold level given below. Sensor image and various threshold lever images:

Figure 3: Sensor image

Figure 4: Threshold level 64

Figure 5: Threshold level 32

Figure 6: Threshold level 16.

4. Conclusion

The proposed reconfigurable PWM architecture for CMOS image sensor has shown promise in terms of robustness in design, high fill factor, good SNR, various array level can be simulated, achieved multiple resolution video coding standard image sensor using high reconfigurable parallel architecture. It can be supported multiple dimension based video codec. Resolution level have been modified by various array processing, the resolution of the image sensor had been depends upon no of pixel i.e. array format can be used 512x512 pixels, 256x256 pixels, 128x128 and also 64x64.The proposed DPWM based Multiple resolution architecture utilize single 2D array of 512x512 matrix for increased resolution without using separable architecture for lower resolutions i.e. above mention pixels.

5. References

1. F. Blais, "Review of 20 years of range sensor development," J. Elect. Imag., vol. 13, no. 1, pp. 231–243, Jan. 2004.
2. P. Seitz, "Quantum-noise limited distance resolution of optical range imaging techniques," IEEE Trans. Circuits Syst. I, vol. 55, no. 8, pp. 2368–2377, Sep. 2008.
3. J. Ohta, Smart CMOS Image Sensors and Applications. Boca Raton, FL, USA: CRC Press, 2008.
4. E. Fossum, "CMOS image sensors: Electronic camera-on-chip," IEEE Trans. Electron Devices, vol. 44, no. 10, pp. 1689–1698, Oct. 1997.
5. S. E. Kemeny, R. Panicacci, B. Pain, L. Matthies, and E. Fossum, "Multiresolution image sensor," IEEE Trans. Circuits Syst. Video Technol., vol. 7, no. 4, pp. 575–583, Aug. 1997.
6. Min-Woong Seo, Shoji Kawahito ,"A Low Dark Leakage Current High-SensitivityCMOS Image Sensor With STI-Less Shared Pixel Design," VOL. 61, NO. 6, JUNE 2014.
7. E. R. Fossum, "CMOS image sensors: Electronic camera-on-a-chip,"IEEE Trans. Electron Devices, vol. 44, no. 10, pp. 1689–1698, Oct. 1997.
8. P. Magnan, "Detection of visible photons in CCD and CMOS: A comparative view," Nucl. Instrum. Methods Phys. Res. A, vol. 504, nos. 1–3, pp. 199–212, 2003.
9. J.-H. Park, S. Aoyama, T. Watanabe, K. Isobe, and S. Kawahito, "A high-speed low-noise CMOS image sensor with 13-b columnparallel single-ended cyclic ADCs," IEEE Trans. Electron Devices, vol. 56, no. 11, pp. 2414–2422, Nov. 2009.