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Implementation of Cuk Converter in Cascaded Multilevel Inverter Using Space Vector Pulse with Modulation Technique

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Abstract:
This paper proposes seven level Space vector pulse width modulation (SVPWM) for a Boost-Buck Cascaded multilevel inverter. This topology requires lesser number of switches, which results in decreased complexity and total cost of the inverter. By applying SVPWM efficiency can be increased due to fundamental frequency switching. In addition to that output harmonic distortions are very much reduced. The numbers are remarkable at power rating and also suitable for the applications of higher temperature. The performance quality in terms of THD and switching losses of the Cascaded Multi level inverter is compared with conventional inverter with reduced number of switching topologies using SVPWM techniques. The circuits are modeled and simulated with help of MATLAB/SIMULINK.

Keywords: *Boost-Buck, Cascaded multilevel inverter, SVPWM, Switching loss reduction, THD.*

1. Introduction

Nowadays, attention has been drawn towards the multilevel inverter to produce good quality of power. Generally, VSI and CSI are widely used for grid integration of energy source. Recently trend goes towards the use of Multilevel inverter generates less output distortion, having lesser common mode voltage, produce less stress, reduces electromagnetic interference due to the above characteristics there is a better quality of output. In recent years, several topologies with various control techniques have been presented for cascaded Multi level inverter [1-4]. In [5] and [7-12] different symmetric cascaded MLI have been presented. The main features of all these structure is the low dc voltage sources, which is the most important advantages in determining the cost of the inverter. MLI have found wide spread applications in the industry, grid integration of renewable energy sources, flexible AC Transmission systems(FACTS) and vehicle propulsion system.

In this paper, in order to increase the number of output voltage levels and the reduced number of switches, driver circuits and the total number of cost of the inverter, NPC is proposed. It is important to note that in the proposed topology, the unidirectional power switches are used. Then to determine the switching angle a SVPWM is proposed, moreover the proposed topology is compared with other topology from different methods such as more number of dc voltage sources, and the value of blocking voltages per switch. Boost-Buck converters when contrasted with different converters, it has the accompanying focal points such that Automatic buck-support operation, Continuous Input and yield current, Localized switching. Finally, the performance of the proposed topology is generating with boost topology levels such as seven level inverters is confirmed by simulating using MATLAB. Various Pulse Width Modulation (PWM) algorithms have been studied to control the multilevel inverter systems and Space Vector Modulation (SVPWM) method is a valid one. The most significant advantages of SVPWM are fast dynamic response and wide linear range of fundamental voltage compared with the conventional PWM. But when it is applied to the diode clamped inverter and flying capacitor inverter, the SVPWM strategy also has to solve the neutral-point voltage unbalance problem.

2. Conventional Method

The block diagram for the conventional method is given below:

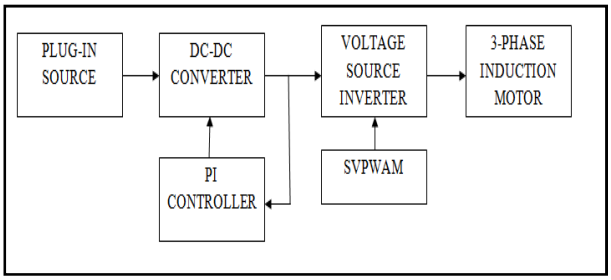

Figure 1: basic block diagram for conventional method

A data voltage is given by module source framework. By then they are redirected to the converter where it is a DC-DC converter which changes over modified voltage to variable voltage. The PI controller in the feedback way controls the yield voltage and it keeps up as enduring by the enacting of switches for diverse plot as showed by the yield voltage so got. By then, the obliged yield voltage is neglected the voltage source inverter and the switches are initiated by the space vector beat width sufficiency conformity framework and it changes over DC to AC and they are disregarded the inciting motor.[13]

3. Proposed Method

The block diagram for the conventional method is given below:

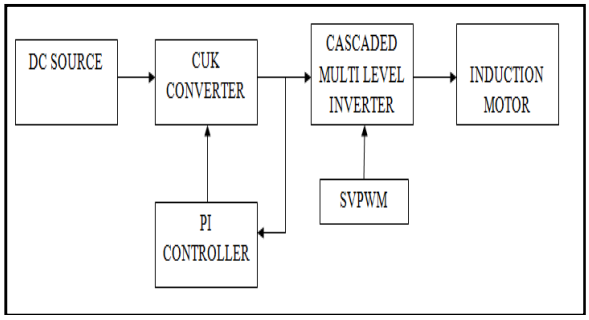

Figure 2: basic block diagram for proposed method

An information voltage is given by module source system. At that point they are diverted to the cuk converter where it is a DC-DC converter which changes over altered voltage to variable voltage. The PI controller in the criticism way controls the yield voltage and it keeps up as steady by the activating of switches for different plot as indicated by the yield voltage so got. At that point the obliged yield voltage is disregarded the Cascaded multilevel inverter and the switches are activated by the space vector beat width sufficiency adjustment system and it changes over DC to AC and they are ignored the prompting engine.[14]-[15]

3.1. Cascaded H Bridge Multi level inverter

In the proposed multilevel inverter During One half cycle of the yield recurrence of 50 Hz the inverter works through three states. PWM gating signs are created by looking at three reference signals (Vref1 ,Vref2 ,and Vref3) with a transporter signal (Carrier).

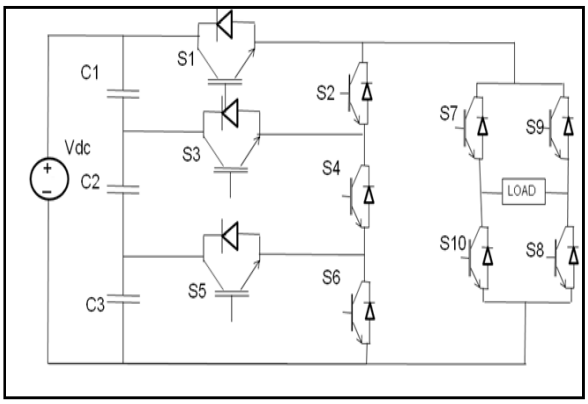

Figure 3: Cascaded Multilevel Inverter

The reference signs have the same recurrence equivalent to line recurrence and same plentifulness. They are in stage with one another with a balance quality equivalent to the sufficiency of the bearer signal. Three reference signs will be contrasted and the bearer signal at once turn by turn. In the event that Vref1 surpasses the crest of the bearer signal V-carrier, Vref2 will take the turn and will be

contrasted and the transporter signal until it surpasses the top of V-carrier. At that point onwards Vref3 will take turn and will be contrasted and bearer signal until it achieves zero. Once Vref3 achieves zero, Vref2 will be looked at again until it achieves zero. The onwards Vref1will be contrasted and Vcarrier. The three states are depicted as takes after

State 1: $\theta < \omega t < \theta 1$ and $\theta 4 < \omega t < \Pi$
State 2: $\theta 1 < \omega t < \theta 2$ and $\theta 3 < \omega t < \theta 4$
State 3: $\theta 2 < \omega t < \theta 3$
The weak list for an inverter is characterized as the proportion of plentifulness of the reference sign to the abundance of transporter sign. Since the proposed inverter PWM regulation procedure uses three bearer flags, the balance list Ma is re-imagined to be
Ma =Am/3Ac
Where Ac is the crest to-top estimation of bearer sign, and Am means the top estimation of voltage reference signal. The exchanging example received in the proposed inverter 2, and the yield voltage levels as indicated by the switch on off.
The gating signs are developed by including shares of the PWM choice signs created by the comparators together through fitting rationale doors. Gating signs for high recurrence switches can be determined to match the yield voltage level indicated. Having the three comparator yields and the yield locales characterized it is conceivable to characterize the exchanging sign for every high recurrence switch. The gating sign for yield extremity generator stage, which changes the extremity of inverter, yield voltage, is straightforward. Low-recurrence yield extremity generator lives up to expectations in two modes: forward and reverse modes. In forward mode, switches S7 and S8 are ON creating positive extremity yield. In converse mode switches S9 and S10 will be ON creating a table

Output Voltage	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**	**S_9**	**S_{10}**
Vdc/3	0	1	0	1	1	0	1	1	0	0
2Vdc/3	0	1	1	0	0	0	1	1	0	0
Vdc	1	0	0	0	0	0	1	1	0	0
0 Vdc	0	1	0	1	0	1	1	1	0	0
-Vdc/3	0	1	0	1	1	0	0	0	1	1
-2Vdc/3	0	1	1	0	0	0	0	0	1	1
-Vdc	1	0	0	0	0	0	0	0	1	1

Table1: switching table of proposed multilevel inverter

3.2. Space Vector Pulse Width Modulation for Multilevel Inverters
Different Pulse Width Modulation (PWM) algorithms have been concentrated on to control the multilevel inverter systems and Space Vector Modulation (Svpwm) method is a substantial one. The most significant advantages of SVPWM are quick dynamic response and wide straight scope of basic voltage compared with the customary PWM. In any case when it is applied to the diode braced inverter and flying capacitor inverter, the SVPWM methodology likewise has to solve the nonpartisan point voltage unbalance problem. There are three fundamental steps to acquire the proper switching states amid each one examining period for the SVPWM technique:

i. Choose the correct fundamental vectors.
ii. Calculate the residence time of every selected vectors.
iii. Select the correct succession of the beat.

3.3. Boost-Buck (Cuk) Converter
A non-separated Cuk converter includes two inductors, a switch which is generally a transistor, and a diode. It is a reversing converter, so the yield voltage is negative concerning the Input voltage. The capacitor C is utilized to exchange vitality and is associated then again to the Input and to the yield of the converter through the replacement of the transistor and the diode. The two inductors L1 and L2 are utilized to change over separately the Input voltage source (Vi) and the yield voltage source (C0) into current sources. Undoubtedly, at a brief time scale an inductor can be considered as a current source as it keeps up a steady present. The transformation is fundamental on the grounds that if the capacitor were associated specifically to the voltage source, the current would be restricted just by (parasitic) safety, bringing about high vitality misfortune. Accusing a capacitor of a current source (the inductor) averts resistive current constraining and its related vitality misfortune. [14]-[15].Likewise with different converters like buck converter, support converter, buck-help converter, the Cuk converter can either work in persistent or spasmodic mode. Be that as it may, not at all like these converters, it can likewise work in irregular voltage mode (i.e. the voltage over the capacitor drops to zero amid the substitution cycle).

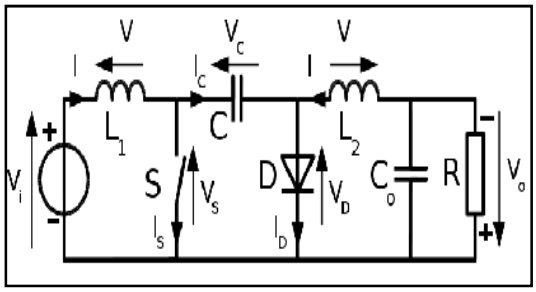

Figure 4: circuit diagram of a Boost-Buck converter

3.4. Operating states of Boost-Buck converter

→ MODE 1: When the switch is open, which is the OFF state, the capacitor C is charged by the Input voltage source through the inductor L1

→ MODE 2: When the switch is shut, which is known as the ON-state; the capacitor C exchanges the vitality to the yield capacitor C0 through the inductance L2.

DESIGN FORMULAS FOR A CUK CONVERTER

To find Duty cycle:

$$\frac{V_{out}}{V_{in}} = \frac{-k}{(1-k)}$$

To find Inductor L1:

$$L_1 = \frac{(1-K)^2 \times R}{2Kf}$$

To find Inductor L2:

$$L_2 = \frac{(1-K)R}{2f}$$

To find capacitor C1:

$$C_1 = \frac{K}{2fR}$$

To find capacitor C2:

$$C_2 = \frac{1}{8fR}$$

where, K-Duty Cycle R-Resistance

a. f-Frequency

b. D.Design Calculation:

To Find Duty cycle K:

Vout	Vin	K
-400	200	0.66

Vout is chosen manually according to required output voltage and find the duty cycle. where, frequency f=25KHzresistance R=8ohms

4. Simulation Result

4.1. Conventional Method

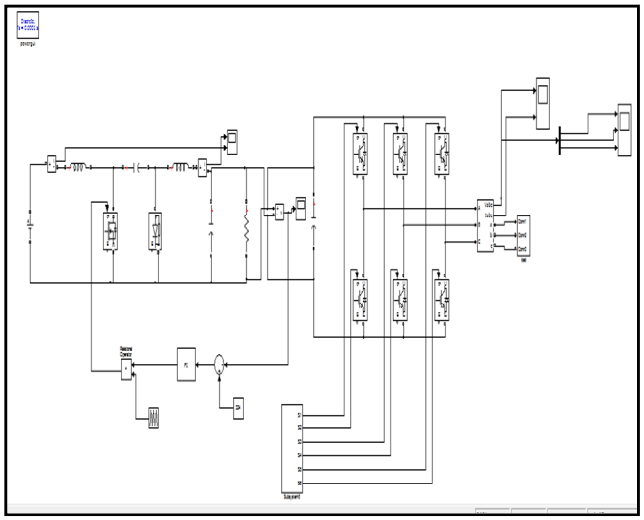

Figure 5: simulation of conventional method

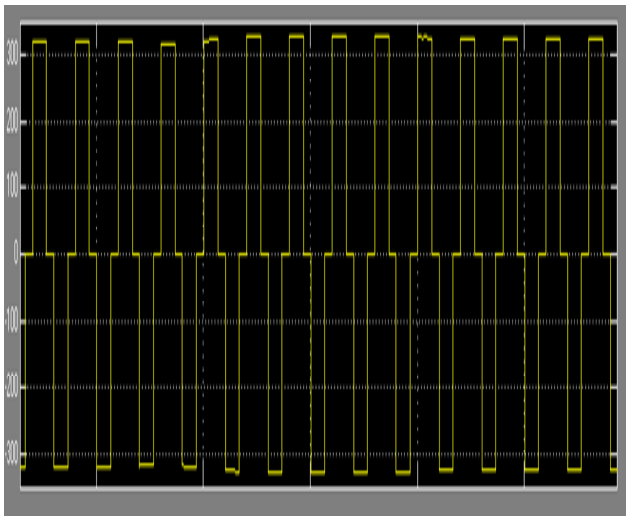

Figure 6: output voltage of VSI inverter

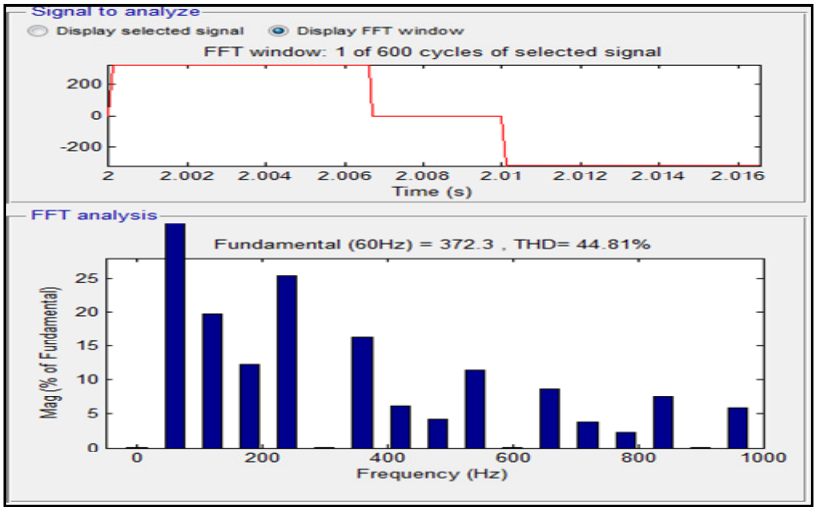

Figure 7: THD for Conventional Method

5. Proposed Method

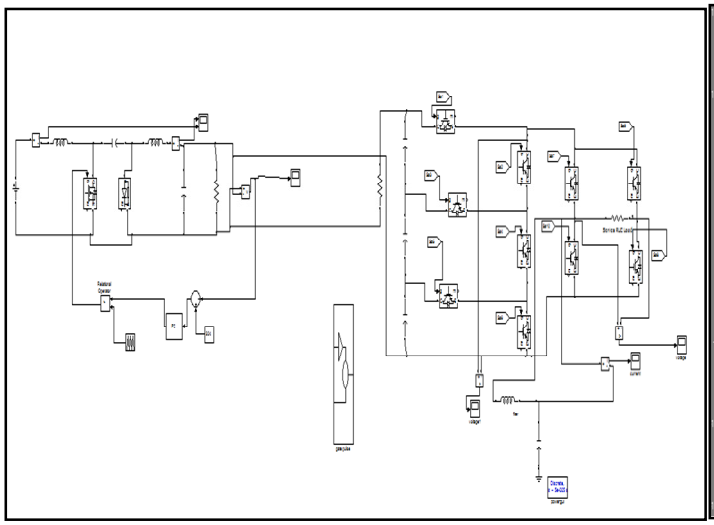

Figure 8: Simulation of proposed multilevel inverter

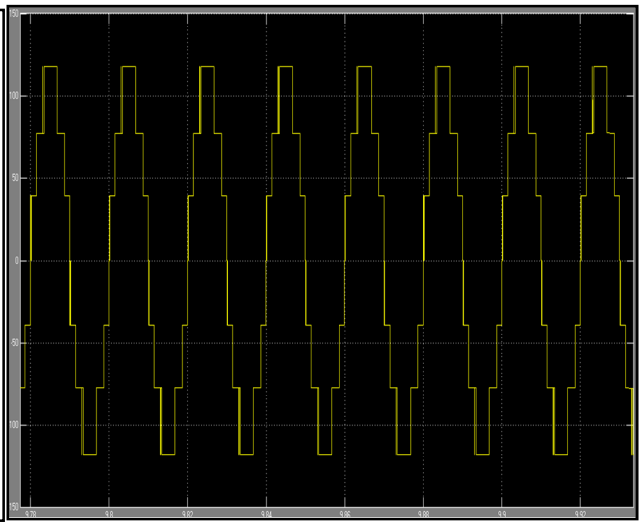

Figure 9: output Voltage of Sevenlevel Inverter

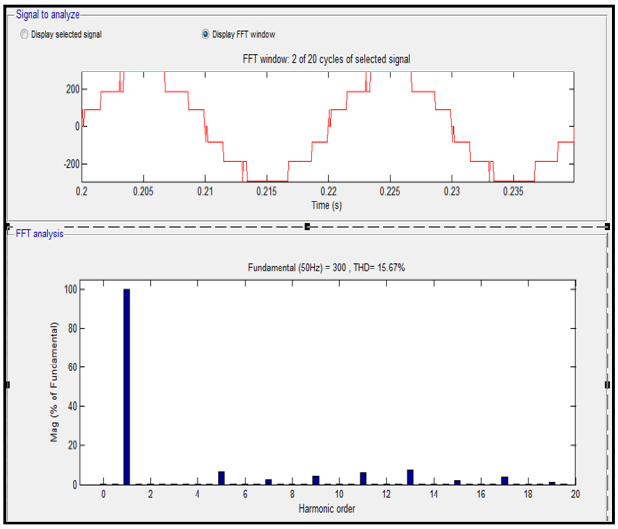

Figure 10: THD of Proposed Inverter

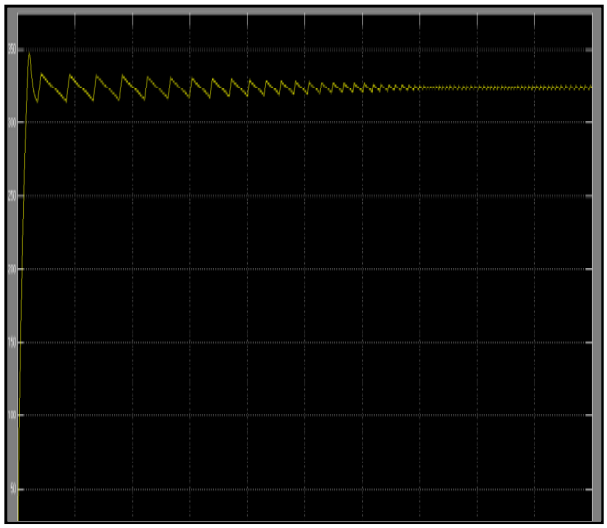

Figure 11: Cuk Converter output

6. Conclusion

In this paper, a new topology with 10 switches introduced and the 7-level output is observed. Circuits are simulated using MATLAB/SIMULINK software and total harmonic distortions are obtained. It can be seen that the conventional topology is better than other presented topology because it requires a lesser number of switch and also THD content is 15.67%lower in comparative result with other mentioned topology.

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